

MA4P7455-1225

Rev. V3

Features

- 4 PIN Diodes in a SOT-25 Plastic Package
- Externally Selectable Bias and RF Matching Network
- 5 4,000 MHz Useable Frequency Band
- 43 dBm IP3 @ 1000 MHz (50 Ω)
- 1 dB Loss @ 1000 MHz (50 Ω)
- 30 dB Attenuation @ 1000 MHz (50 Ω)
- Lead-Free SOT-25 Package
- RoHS* Compliant Version of MA4P274-1225

Applications

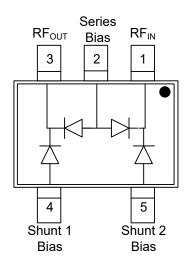
CATV / Broadband

Description

The MA4P7455-1225 is a wideband, lower insertion loss, high IP3, Quad PIN diode π Attenuator in a lead free surface mount SOT-25 package. Four PIN diodes in one package reduce design parasitics and improve circuit density.

These PIN diode attenuators perform well where RF signal amplitude control is required in 50 Ω handset circuits and 75 Ω broadband CATV systems. Exceptional insertion loss, attenuation range, and IP3 at <10 mA bias make these devices suitable for better power level control in RF amplifiers.

Functional Schematic



Pin Configuration

Pin #	Function	
1	RF Input	
2	Series Bias	
3	RF Output	
4	Shunt 1 Bias	
5	Shunt 2 Bias	

Ordering Information¹

Part #	Package
MA4P7455-1225T	Tape & Reel
MADP-007455-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.

^{*} Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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Typical 50 Ω Performance²: 1000 MHZ @ 25°C using Wideband RF Circuit Design

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Insertion Loss	3.0 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias	dB		-2	—
Insertion Loss	6.5 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias	dB		-1	
Return Loss	6.5 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias	dB		-10	
Attenuation	0 mA - Series Diode Bias / 0.75 V - Shunt 1 and 2 Bias	dB		-29	
Input IP3	0 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias 6.5 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias F1 = 1000 MHz, F2 = 1100 MHz	dBm		43 43	
Input IP3	0 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias 6.5 mA Series Diode Bias / 0.75 V Shunt 1 and 2 Bias F1 = 100 MHz, F2 = 110 MHz	dBm		43 33	_
Settling Time	Within 1 dB of Final Attenuation Value	uS	_	3	_
RF C.W. Incident Power	0 - 20 V Series Diode Bias / 0.75 V Shunt 1 and 2 Bias	dBm	—	+20	—

Typical 75 Ω Performance²: 1000 MHZ @ 25°C using Wideband RF Circuit Design

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Insertion Loss	2.0 mA Series Diode Bias / 1 V Shunt 1 and 2 Bias 4.5 mA Series Diode Bias / 1 V Shunt 1 and 2 Bias	dB	_	-1.1 -0.6	_
Attenuation	0 mA / Series Diode and 1 V Shunt 1 and 2 Bias	dB	_	-27	—
Return Loss	4.5 mA / Series Diode and 1 V Shunt 1 and 2 Bias	dB	—	-10	—

2. Values shown include through loss calibrated out of RF test circuit.

Absolute Maximum Ratings^{3,4}

Parameter	Absolute Maximum	
DC Current	75 mA	
DC Voltage at Temperature Extremes	- 100 V	
Operating Temperature	-65 °C to +125 °C	
Storage Temperature (No Dissipated Power)	-65 °C to +150 °C	

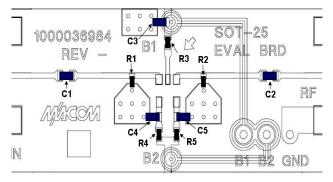
3. Exceeding any one or combination of these limits may cause permanent damage to this device.

4. M/A-COM does not recommend sustained operation near these survivability limits.

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Recommended PCB Layout



Parts List

Part	Value	Case Style	Manufacturer
C1 - C5	100 pF	0603	Murata
R1 - R5	1000 Ω	0402	Panasonic

Spice Model

Pin Diode Model NLPINM2 Is = 1E-14 A Vi = 0 V Un = 900 cm ² /V-sec Wi = 60 um Rr = 1.25 Ohm Cmin = 0.20 pF Tau = 1.0 usec Rs = 0.1 Ohm Cjo = 0.27 pF Vj = 0.7 V M = 0.5 Fc = 0.5 Imax = 2.5E+6 A/m ² Kf = 0 Af = 1 Ffe = 1 wBV = 150 V
WDV - 150 V

Series & Shunt Diode Bias Currents as a Function of Vseries & Vshunt Voltage (Values shown are PER DIODE)

Vshunt Bias (V)	Vseries Bias (V)	lseries Diode (mA)	lshunt Diode (mA)
0.75	0	0.000	0.192
0.75	1	0.106	0.120
0.75	2	0.443	0.048
0.75	3	0/773	0
0.75	4	1.099	0
0.75	5	1.426	0
0.75	6	1.750	0
0.75	7	2.092	0
0.75	8	2.424	0
0.75	9	2.756	0
0.75	10	3.088	0
0.75	11	3.421	0
0.75	12	3.754	0
0.75	13	4.087	0
0.75	14	4.410	0
0.75	15	4.743	0
0.75	16	5.081	0
0.75	17	5.406	0
0.75	18	5.750	0
0.75	19	6.079	0
0.75	20	6.413	0

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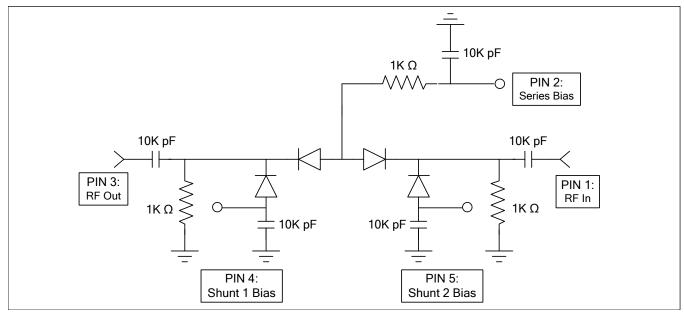
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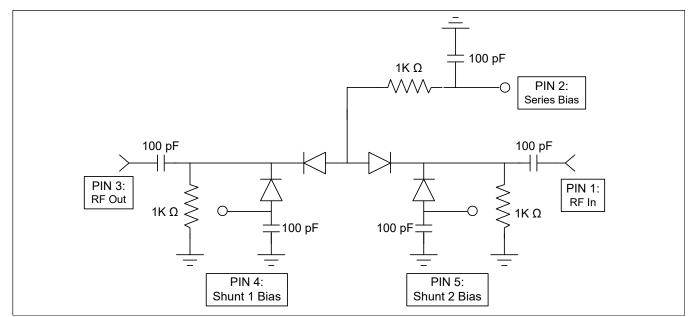
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Schematic 5 - 1000 MHz, 50 Ω, RF Circuit⁵



5. Keeping pin 4 & pin 5 as separate bias points (same V) reduces RF leakage (increases attenuation) through an otherwise connected common anode bias note.

Schematic 1 - 4 GHz, 50 Ω, RF Circuit⁶



6. Keeping pin 4 & pin 5 as separate bias points (same V) reduces RF leakage through an otherwise connected common anode bias node.

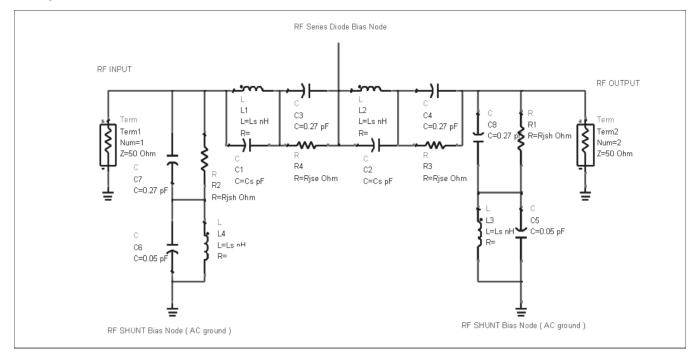
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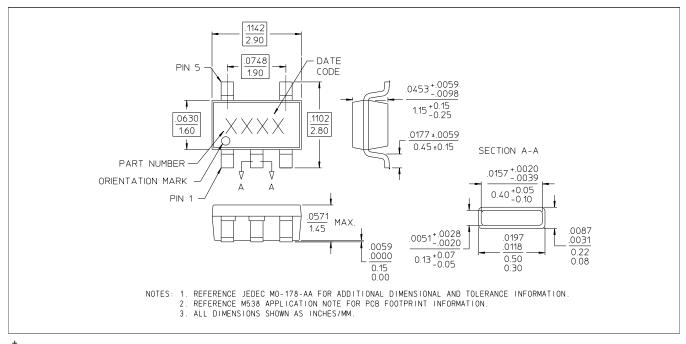
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Lumped Element Model for MA4P7455-1225 PIN Diode π Attenuator in SOT-25



Lead Free SOT-25[†]



[†] Reference Application Note M538 for lead-free solder reflow recommendations. Meets JEDEC moisture sensitivity level 1 requirements.

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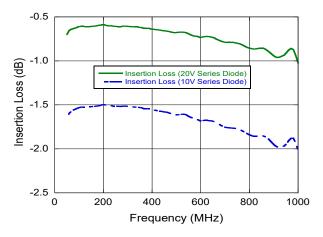


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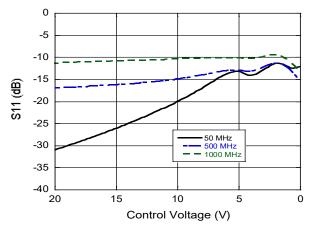
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Typical Performance Curves @ +25°C, 50 - 1000 MHz, Shunt Bias = 0.75 Volts

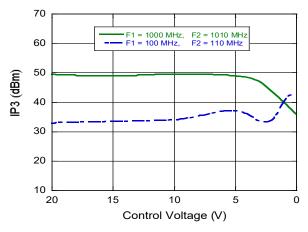
Insertion Loss vs. Frequency



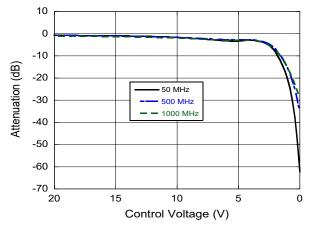
Input Return Loss vs. Control Voltage



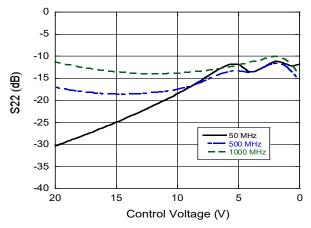
IP3 vs. Control Voltage



Attenuation vs. Control Voltage



Output Return Loss vs. Control Voltage

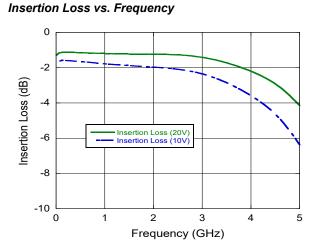


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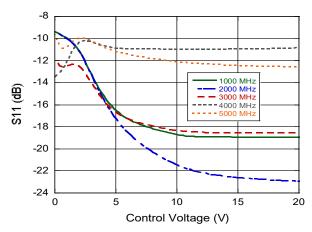


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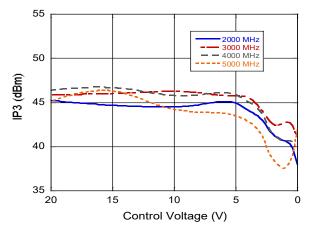
Typical Performance Curves @ +25°C, 1000 - 5000 MHz, Shunt Bias = 0.75 Volts



Input Return Loss vs. Control Voltage

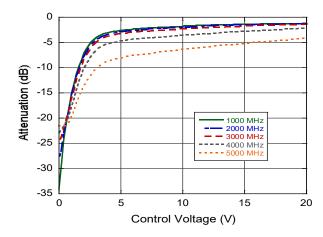


IP3 vs. Control Voltage (10 MHz Spacing)

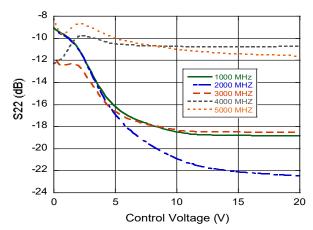


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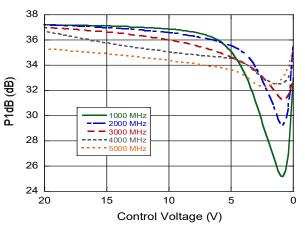
Attenuation vs. Control Voltage



Output Return Loss vs. Control Voltage







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